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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,467	04/11/2001	Michael McLoughlin	SRT-024	4529

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 01/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,467	MCLOUGHLIN ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/11/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *response to arguments*.

DETAILED ACTION

1. Claims 1-9, 11-17, 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Petivan et al. U.S. Patent 6,141,769, as cited in prior office action, which was mailed on 8/3/2004.

2. Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petivan, as cited in prior office action, which was mailed on 8/3/2004.

3. Claims 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Petivan et al. U.S. Patent 6,141,769.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 11-17, 19-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Petivan et al. U.S. Patent 6,141,769.

As per claim 1, Petivan teaches a fault-tolerant server comprising: (a) a communications link (figure 3); (b) a first Central Processing Unit (CPU) in electrical communication with the communications link (abstract) and capable of transmitting a first information stream (column 3, lines 4-25; figure 2); (c) a second CPU in electrical communication with the communications link (abstract) and capable of transmitting a second information stream (column 3, lines 4-25; figure 2); (d) a first Input/Output (I/O) subsystem in electrical communication with the first CPU and with the communications link, configured to compare the first information stream and the second information stream (column 3, lines 53-67)); and (e) a first local mass storage device in electrical communication with the first I/O subsystem (figure 2; column 3, lines 4-8), wherein the first I/O subsystem selectively accesses the first local mass storage device in response to a comparison of the first and second information streams (column 42, lines 27-34; column 10, lines 5-38).

As per claim 2, Petivan teaches the fault-tolerant server of claim 1 further comprising a second Input/Output (I/O) subsystem in electrical communication with the second CPU and with the communications link, configured to compare the first information stream and the second information stream (figure 2; column 3, lines 2-8); and second local mass storage device in electrical communication with the second I/O subsystem (figure 2; column 3, lines 2-8), wherein the second I/O subsystem selectively accesses the second local mass storage device in response to a comparison of the first and second information (column 42, lines 27-34; column 10, lines 5-38).

As per claim 3, Petivan teaches the fault-tolerant server of claim 2 wherein at least one of the first I/O subsystems and the second I/O subsystem are in electrical communication with at

least one of the first local mass storage device and the second local mass storage device (column 3, lines 2-8; figure 2).

As per claim 4, Petivan teaches the fault-tolerant server of claim 2 wherein the communications link comprises a respective switching fabric in electrical communication with the respective CPU (column 3, lines 18-20).

As per claim 5, Petivan teaches the fault-tolerant server of claim 4 wherein the switching fabric is in electrical communication with at least one of the first I/O subsystem and the second I/O subsystem (column 3, lines 18-20).

As per claim 6, Petivan teaches the fault-tolerant server of claim 5 wherein the switching fabric is in electrical communication with the other one of the first I/O subsystem and the second I/O subsystem (column 3, lines 18-20).

As per claim 7, Petivan teaches the fault-tolerant server of claim 1 further comprising a delay module in electrical communication with at least one of the first I/O subsystem and the second I/O subsystem to delay transmission of at least one of the first and second information streams (column 9, lines 18-22; figure 2; column 3, lines 2-8).

As per claim 8, Petivan teaches the fault-tolerant server of claim 1 wherein the communications link comprises a backplane (column 2, lines 48-50).

As per claim 9, Petivan teaches the fault-tolerant server of claim 8 wherein the communications link further comprises a backplane link in communication with the backplane (column 2, lines 48-50).

As per claim 11, Petivan the fault-tolerant server of claim 1 wherein the first local mass storage device is located on a same motherboard as the first CPU (column 2, lines 39-41; figure 2).

As per claim 12, Petivan the fault-tolerant server of claim 1 wherein the second local mass storage device is located on a same motherboard as the second CPU (figure 2; column 2, lines 39-41).

As per claim 13, Petivan a method for accessing at least one of a first local mass storage device and a second local mass storage device in a fault-tolerant server, the method comprising the steps of: (a) establishing communication between a first Central Processing Unit (CPU) and a first local mass storage device capable of transmitting a first information stream; (b) establishing communication between a second CPU and a second local mass storage device capable of transmitting a second information stream (abstract; figure 2; column 3, lines 4-25); and (c) comparing the first information stream and the second information stream through the use of a first Input/Output (I/O) subsystem, in communication with the first CPU and the first local mass storage device; and (d) selectively accessing, by the first I/O subsystem, the first local mass storage device in response to a comparison of the first and second information (column 42, lines 27-34; column 10, lines 5-38).

As per claim 14, Petivan the method of claim 13 further comprising the steps of (e) comparing the first information stream and the second information stream through the use of the second Input/Output (I/O) subsystem, in communication with the second CPU and the second local mass storage device (column 3, lines 2-8; figure 2), and (f) selectively accessing, by the

second I/O subsystem, the second local mass storage device in response to a comparison of the first and second information streams streams (column 42, lines 27-34; column 10, lines 5-38).

As per claim 15, Petivan the method of claim 14 further comprising storing a datum in one of the first local mass storage device and the second local mass storage device (column 9, lines 52-53), and storing the datum in the other one of the first local mass storage device and the second local mass storage device by mirroring software (column 14, lines 40-46).

As per claim 16, Petivan the method of claim 13 further comprising the step of communicating with a backplane (column 2, lines 48-50).

As per claim 17, Petivan the method of claim 13 further comprising introducing a parity bit to detect an error in the established communication (column 4, lines 25-29; column 12, lines 3-8).

As per claim 19, Petivan the method of claim 13 further comprising the step of communicating with at least one of the first I/O subsystem and the second I/O subsystem over a switching fabric (column 3, lines 18-20).

As per claim 20, Petivan the method of claim 14 further comprising the step of delaying the accessing of at least one of the first local mass storage device and the second local mass storage device (column 9, lines 18-22).

As per claim 21, Petivan an apparatus for accessing at least one of a first local mass storage device and a second local mass storage device in a fault-tolerant server, the apparatus comprising: (a) a means for establishing communication between a first Central Processing Unit (CPU) and a first local mass storage device capable of transmitting a second information stream; (b) a means for establishing communication between a second CPU and a second local mass

storage device capable of transmitting a second information stream (abstract; figure 2; column 3, lines 4-25); (c) a first Input/Output subsystem means, in communication with the first CPU and the first local mass storage device, configured to compare the first information stream and the second information stream (column 3, lines 53-67); and (d) a means for selectively accessing, by the first I/O subsystem, the first local mass storage device in response to a comparison of the first and second information streams streams (column 42, lines 27-34; column 10, lines 5-38).

As per claim 22, Petivan teaches the method of claim 13 further comprising the step of executing the second CPU in lockstep with the first CPU (column 3, lines 62-67).

As per claim 23, Petivan teaches a server comprising a communications link (figure 3); a first Central Processing Unit, (CPU), in electrical communication with the communications link and capable of transmitting a first information stream; a second CPU in electrical communication with the communications link and capable of transmitting a second information stream (column 3, lines 4-25); a first Input/output (I/0) subsystem, in electrical communication with the first CPU and with the communications link, configured to compare the first information stream and the second information stream; a first local mass storage device in electrical communication with the first I/0 subsystem (column 3, lines 4-67); a second Input/output (I/0) subsystem, in electrical communication with the second CPU and with the communications link, configured to compare the first information stream and the second information stream; and a second local mass storage device in electrical communication with the second I/0 subsystem (column 3, lines 2-8), wherein at least one of the first I/0 subsystem and the second I/0 subsystem selectively accesses at least one of the first local mass storage device and the second local mass storage device in response to

a comparison of the first and second information streams streams (column 42, lines 27-34; column 10, lines 5-38).

As per claim 24, Petivan teaches a method for accessing at least one of a first local mass storage device and a second local mass storage device in a fault-tolerant server, the method comprising the steps of establishing communication between a first Central Processing Unit (CPU) and a first local mass storage device capable of transmitting a first information stream (column 3, lines 4-67); establishing communication between a second CPU and a second local mass storage device capable of transmitting a second information stream (column 3, lines 2-8); comparing the first information stream and the second information stream through the use of a first Input/output (I/0) subsystem, in communication with the first CPU and the first local mass storage device (column 3, lines 53-67); comparing the first information stream and the second information stream through the use of a second Input/output (I/0) subsystem, in communication with the second CPU and the second local mass storage device (column 3, lines 2-8); and selectively accessing, by at least one of the first 1/0 subsystem and the second I/0 subsystem, at least one of the first local mass storage device and the second local mass storage device, in response to a comparison of the first and second information streams streams (column 42, lines 27-34; column 10, lines 5-38).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petivan.

As per claims 10 and 18, Petivan does not specifically disclose the first CPU and the second CPU to further comprise a 1U rack-mount motherboard and the step of communicating therein. However, rack-mounting equipment is notoriously well known in the art. Examiner takes Official Notice for a 1U rack-mount form factor circuitry, such circuitry comprising a motherboard. A person of ordinary skill in the art at the time of the invention would have been motivated to use a 1U rack-mount form factor because he would not want to simply put the equipment on a shelf, it provides a more manageable footprint, it looks professional and industrial, and because it is a matter of design.

Response to Arguments

6. Applicant's arguments filed 12/2/2004 have been fully considered but they are not persuasive.

Applicants have argued that Petivan teaches only wherein the information written to the target I/O device can only originate from the processor local to that target I/0 device, and Petivan prohibits providing information from a processor to a target I/0 device local to any other processor. The examiner respectfully disagrees. Petivan teaches in column 37, lines 27-53 that any processor can read each other's registers to share information local to the respective processor.

Applicants have argued that Petivan does not teach a system wherein the first I/0 subsystem selectively accesses the first local mass storage device in response to a comparison of the first and second information streams. The examiner respectfully disagrees. Petivan teaches that during a transaction, e.g. a write transaction (column 42, lines 27-34), the control, address, and data signals are compared concurrently with the accessing transaction. If a mismatch during a compare occurs, the accessing of the local device is interrupted (column 10, lines 5-34). Thus, when an executing processor is actively accessing the local device, the accessing is interrupted by the compare error (column 10, lines 35-38). Therefore, in response to a mismatch of the comparison of the information streams among the modules, the selective accessing of the local device is effected. The examiner interprets the term of selectively accessing as either accessing or the discontinuance of accessing. This teaches the limitation of selectively accessing a local device in response to the comparison of at least a first and second information stream. Therefore, all rejected claims stand.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
January 26, 2005

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